

Notice of References Cited	Application/Control No. 10/695,609	Applicant(s)/Patent Under Reexamination IINO ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	A	US-5,911,822	06-1999	Abe et al.	117/13
X	B	US-5,501,172	03-1996	Murai et al.	117/15
X	C	US-6,461,582 B2	10-2002	Weber et al.	423/328.2
X	D	US-2002/0000188 A1	01-2002	Weber et al.	117/13
X	E	US-2003/0033972 A1	02-2003	Javidi, Massoud	117/13
X	F	US-2002/0000187 A1	01-2002	IINO, EIICHI	117/13
X	G	US-6,670,036 B2	12-2003	Iino et al.	428/402
X	H	US-6,315,970 B1	11-2001	Iino, Eiichi	423/328.1
X	I	US-6,210,477 B1	04-2001	Izumi et al.	117/35
X	J	US-6,197,108 B1	03-2001	Iino et al.	117/13
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf et al., Silicon Processing for the VLSI Era, Volume 1: Process Technology, Sunset Press, CA, USA, pp. 59-61, 1986.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Matthew Anderson 4/13/2005